CLAIMS

1. In a memory device:

at least one memory array containing a plurality of memory cells arranged in rows and columns;

a DC sense amplifier having first and second inputs and an output coupled to an externally accessible data terminal of the memory device;

a pair of I/O lines coupled to the inputs of the DC sense amplifier;

a plurality of pairs of complementary digit lines for each column that may be coupled to the pair of I/O lines; and

a test circuit for facilitating the testing of the memory device, the testing circuit selectively operating in either a normal mode or a test mode, the testing circuit, when operating in the normal mode, coupling the inputs of the DC sense amplifier to the pair of digit lines for one column of the array, and the testing circuit, when operating in the test mode, coupling one of the inputs of the DC sense amplifier to a first plurality of digit lines of the array and another of the inputs of the DC sense amplifier to a second plurality of digit lines for the array.

2. The memory device of claim 1 wherein the second plurality of digit lines comprise complements of the first plurality of digit lines.

3. The memory device of claim 1, further comprising a NOR gate having a first input coupled to the first input of the DC sense amplifier and a second input coupled to the second input of the DC sense amplifier, an output of the NOR gate indicating a failed memory cell when both inputs to the NOR gate are at logic "0."

4. The memory device of claim 1, further comprising:

a first weak latch coupled to the first input of the DC sense amplifier; and

a second weak latch coupled to the second input of the DC sense amplifier.

5. The memory device of claim 1 wherein the DC sense amplifier comprises:

a first current mirror amplifier having an input coupled to the first input of the DC sense amplifier and having first and second outputs;

a second current mirror amplifier having an input coupled to the second input of the DC sense amplifier and having first and second outputs;

a third current mirror amplifier having a first input coupled to the first output of the first current mirror amplifier and an output coupled to the first output of the second current mirror amplifier and to a first output of the DC sense amplifier; and

a fourth current mirror amplifier having a first input coupled to the second output of the first current mirror amplifier and an output coupled to the second output of the second current mirror amplifier and to a second output of the DC sense amplifier.

6. The test circuit of claim 1 wherein the columns for the digit lines that the switching circuit couples to inputs of the DC sense amplifier in the test mode are in different arrays of the memory device.

7. The test circuit of claim 1 wherein the switching circuit comprises a plurality of pass gates coupling the pair of I/O lines to a pair of complementary digit lines for a first array and a pair of complementary digit lines for a second array.

8. The test circuit of claim 1 wherein the switching circuit comprises a plurality of pass gates coupling the pair of I/O lines to a pair of complementary digit lines for a first column and a pair of complementary digit lines for a second column.

9. The test circuit of claim 1 wherein the memory device comprises a dynamic random access memory.

10. The memory device of claim 1 wherein, in the test mode, the switching circuit couples complementary digit lines for the first and second arrays corresponding to memory cells in the first and second arrays that are both replaceable as a group by rows or columns of redundant or spare memory cells.

11. The memory device of claim 1 wherein the DC sense amplifier comprises:

a first differential amplifier having an input coupled to the first input of the DC sense amplifier and first and second outputs each having a gain of α_1;

a second differential amplifier having an input coupled to the second input of the DC sense amplifier and first and second outputs each having a gain of α_1; and

a third differential amplifier having a first input coupled to the first output of the first differential amplifier and an output coupled to the second output of the second differential amplifier, the third differential amplifier configured to provide a gain of α_2 and an output signal coupled to a first output of the DC sense amplifier that is α_1 times the signal at the first input of the DC sense amplifier minus $\alpha_1\alpha_2$ times the signal at the second input of the DC sense amplifier.

12. The memory device of claim 11, further comprising a fourth differential amplifier having a first input coupled to the second output of the first differential amplifier and an output coupled to the first output of the second differential amplifier, the fourth differential amplifier configured to provide a gain of α_2 and an output signal coupled to a second output of the DC sense amplifier that is α_1 times the signal at the second input of the DC sense amplifier minus $\alpha_1\alpha_2$ times the signal at the first input of the DC sense amplifier.

13. In a memory device:

at least one memory array containing a plurality of memory cells arranged in rows and columns;

a DC sense amplifier having first and second inputs and an output coupled to an externally accessible data terminal of the memory device;

a pair of I/O lines coupled to the inputs of the DC sense amplifier;

a plurality of pairs of complementary digit lines for each column that may be coupled to the pair of I/O lines; and

a test circuit for facilitating the testing of the memory device, comprising:

a switching circuit coupled between the inputs of the DC sense amplifier and a pair of digit lines for one column of the array and between the inputs of the DC sense amplifier and a pair of digit lines for another column of the array, the switching circuit selectively operating in either a normal mode or a test mode, the switching circuit, when operating in the normal mode, coupling the inputs of the DC sense amplifier to the pair of digit lines for one column of the array, and the switching circuit, when operating in the test mode, coupling one of the inputs of the DC sense amplifier to a first plurality of pairs of digit lines of the array and another of the inputs of the DC sense amplifier to a second plurality of pairs of digit lines for the array; and

a NOR gate having a first input coupled to the first input of the DC sense amplifier and a second input coupled to the second input of the DC sense amplifier, an output of the NOR gate indicating a failed memory cell when both inputs to the NOR gate are at logic "0."

14. The memory device of claim 13 wherein the second plurality of digit lines comprise complements of the first plurality of pairs of digit lines.

15. The memory device of claim 13, further comprising:

a first weak latch coupled to the first input of the direct sense amplifier; and

a second weak latch coupled to the second input of the direct sense amplifier.

16. The memory device of claim 13 wherein the DC sense amplifier comprises:

a first current mirror amplifier having an input coupled to the first input of the DC sense amplifier and having first and second outputs;

a second current mirror amplifier having an input coupled to the second input of the DC sense amplifier and having first and second outputs;

a third current mirror amplifier having a first input coupled to the first output of the first current mirror amplifier and an output coupled to the first output of the second current mirror amplifier and to a first output of the DC sense amplifier; and

a fourth current mirror amplifier having a first input coupled to the second output of the first current mirror amplifier and an output coupled to the second output of the second current mirror amplifier and to a second output of the DC sense amplifier.

17. The test circuit of claim 13 wherein the columns for the digit lines that the switching circuit couples to inputs of the DC sense amplifier in the test mode are in different arrays of the memory device.

18. The test circuit of claim 13 wherein the switching circuit comprises a plurality of pass gates coupling the pair of I/O lines to a pair of complementary digit lines for a first array and a pair of complementary digit lines for a second array.

19. The test circuit of claim 13 wherein the switching circuit comprises a plurality of pass gates coupling the pair of I/O lines to a pair of complementary digit lines for a first column and a pair of complementary digit lines for a second column.

20. The test circuit of claim 13 wherein the memory device comprises a dynamic random access memory.

21. The memory device of claim 13 wherein, in the test mode, the switching circuit couples complementary digit lines for the first and second arrays corresponding to memory cells in the first and second arrays that are both replaceable as a group by rows or columns of redundant or spare memory cells.

22. The memory device of claim 13 wherein the DC sense amplifier comprises:

a first differential amplifier having an input coupled to the first input of the DC sense amplifier and first and second outputs each having a gain of α_1;

a second differential amplifier having an input coupled to the second input of the DC sense amplifier and first and second outputs each having a gain of α_1; and

a third differential amplifier having a first input coupled to the first output of the first differential amplifier and an output coupled to the second output of the second differential amplifier, the third differential amplifier configured to provide a gain of α_2 and an output signal coupled to a first output of the DC sense amplifier that is α_1 times the signal at the first input of the DC sense amplifier minus $\alpha_1\alpha_2$ times the signal at the second input of the DC sense amplifier.

23. The memory device of claim 22, further comprising a fourth differential amplifier having a first input coupled to the second output of the first differential amplifier and an output coupled to the first output of the second differential amplifier, the fourth differential amplifier configured to provide a gain of α_2 and an output signal coupled to a second output of the DC sense amplifier that is α_1 times the signal at the second input of the DC sense amplifier minus $\alpha_1\alpha_2$ times the signal at the first input of the DC sense amplifier.

24. A memory device having an address bus and a data terminal, comprising:

at least one array of memory cells arranged in rows and columns, each of the rows having a row line and each of the columns having a pair of complementary digit lines;

a row address circuit coupled to the address bus for activating a row line corresponding to a row address coupled to the row address circuit through the address bus;

a column address circuit coupled to the address bus for coupling to a pair of I/O lines a pair of digit lines for a column corresponding to a column address coupled to the column address circuit through the address bus;

a DC sense amplifier having a pair of inputs and an output coupled to the data terminal of the memory device; and

a switching circuit operating in a normal mode to couple the inputs of the DC sense amplifier to a pair of digit lines for the same column and operating in a test mode to couple the inputs of the DC sense amplifier to a plurality of digit lines for different columns.

25. The memory device of claim 24 wherein the different columns are in different arrays of the memory device.

26. The memory device of claim 24 wherein the memory device comprises a dynamic random access memory.

27. The memory device of claim 24, further comprising a NOR gate having a first input coupled to the first input of the DC sense amplifier and a second input coupled to the second input of the DC sense amplifier, an output of the NOR gate indicating a failed memory cell when both inputs of the NOR gate are in the same logical state.

28. The memory device of claim 27 wherein, in the test mode, the switching circuit couples I/O lines for first and second arrays corresponding to memory cells in the first and second arrays that are replaceable as a group by rows or columns of redundant memory cells.

29. A memory device having an address bus and a data terminal, comprising:

first and second arrays of memory cells in which the memory cells in each array are arranged in rows and columns, each of the rows having a row line and each of the columns having a pair of complementary digit lines;

a row address circuit coupled to the address bus for activating a row line in one of the arrays corresponding to a row address applied to the row address circuit through the address bus;

a column address circuit coupled to the address bus for coupling a respective pair of I/O lines for each array to a pair of digit lines corresponding to a column address applied to the column address circuit through the address bus;

a DC sense amplifier having a pair of inputs coupled to the pair of I/O lines and an output coupled to the data terminal of the memory device; and

a switching circuit operating in a normal mode to couple the I/O lines for either the first or the second arrays to the complementary digit lines and operating in a test mode to couple each of the I/O lines for the first array to the complementary digit lines and to couple each of the I/O lines for the second array to the complementary digit lines.

30. The memory device of claim 29 wherein the memory device comprises a dynamic random access memory.

31. The memory device of claim 29, further comprising combinatorial logic having a first input coupled to a first of the pair of inputs to the DC sense amplifier and a second input coupled to a second of the pair of inputs to the

DC sense amplifier, the combinatorial logic providing an output signal indicative of a defective memory cell when both the first and second inputs to the DC sense amplifier are in the same logical state.

32. The memory device of claim 29 wherein, in the test mode, the switching circuit couples digit lines for the first and second arrays corresponding to memory cells in the first and second arrays that are replaceable as a group by rows or columns of redundant memory cells.

33. A system for testing a memory device having an array of memory cells arranged in rows and columns, each of the columns having a pair of complementary digit lines, addressing circuits coupled to an address bus for selecting memory cells to which data are written and from which data are read, and a DC sense amplifier having an output coupled to a data terminal of the memory device, the test system comprising:

a multiplexer included in the memory device, the multiplexer being controlled by a mode signal to operate in either a normal mode or a test mode, the multiplexer operating in the normal mode to couple digit lines of the same column to respective inputs of the DC sense amplifier and operating in a test mode to couple digit lines of a plurality of columns to respective inputs of the DC sense amplifier;

a mode control circuit included in the memory device, the mode control circuit having an output terminal and a plurality of input terminals coupled to externally accessible input terminals of the memory device, the mode control circuit generating a mode control signal to cause the multiplexer to operate in the normal mode responsive to a first combination of signals applied to the externally accessible input terminals and generating a mode control signal to cause the multiplexer to operate in the test mode responsive to a second combination of signals applied to the externally accessible input terminals; and

a testing device external to the memory device, the testing device including addressing circuits for applying addresses to the address bus of the memory

device, a mode controller for selectively applying the first and second combinations of signals to the externally accessible input terminals of the memory device, a data generating circuit to apply background data to the data terminal of the memory device, and a data analyzing circuit for examining read data coupled from the data terminal of the memory device in the test mode to determine if the read data corresponds to the write data.

34. The test system of claim 33 wherein the different columns for which the digit lines are coupled to the inputs of the DC sense amplifier in the test mode are in different arrays of the memory device.

35. The test system of claim 33 wherein the memory device comprises a dynamic random access memory.

36. The test system of claim 33 wherein the memory device further comprises a NOR gate having a first input coupled to the first input of the DC sense amplifier and a second input coupled to the second input of the DC sense amplifier, so that, when the multiplexer is in the test mode, an output of the NOR gate indicates a defective memory cell when the first and second inputs to the NOR gate are in the same logical state.

37. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus and adapted to allow data to be output from the computer system; and

a memory device coupled to the processor through the processor bus, the memory device comprising:

at least one array of memory cells arranged in rows and columns, each of the rows having a row line and each of the columns having a pair of complementary digit lines;

a row address circuit adapted to receive and decode a row address, and to select a row of memory cells corresponding to the row address;

a column address circuit adapted to couple a pair of digit lines for a column corresponding to a column address to a pair of I/O lines to receive or apply data to one of the memory cells in the selected row corresponding to a column address;

a data path circuit adapted to couple data between an external data terminal and each of a plurality of pairs of complementary digit lines for respective columns; the data path circuit including a DC sense amplifier having a pair of inputs and an output coupled to the external data terminal of the memory device; and

a multiplexer operating in a normal mode to couple the inputs of the DC sense amplifier through a pair of the I/O lines to a pair of digit lines for the same column and operating in a test mode to couple the inputs of the DC sense amplifier through a pair of the I/O lines to a plurality of pairs of digit lines for different columns.

38. The computer system of claim 37 wherein the different columns for which the digit lines are coupled to the inputs of the DC sense amplifier in the test mode are in different arrays of the memory device.

39. The computer system of claim 37 wherein the memory device comprises a dynamic random access memory.

40. The computer system of claim 37, further comprising a NOR gate having inputs coupled to the digit lines, an output of the NOR gate indicating a defective memory cell when both digit lines are at logical "0."

41. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device coupled to the processor through the processor bus, the memory device comprising:

first and second arrays of memory cells in which the memory cells in each array are arranged in rows and columns, each of the rows having a row line and each of the columns having a pair of complementary digit lines;

a row address circuit coupled to the address bus for activating a row line in one of the arrays corresponding to a row address applied to the row address circuit through the address bus;

a column address circuit coupled to the address bus for coupling a respective pair of I/O lines for each array to a pair of digit lines corresponding to a column address applied to the column address circuit through the address bus;

a data path circuit adapted to couple data between an external data terminal and each of a plurality of pairs of complementary digit lines for respective columns, the data path circuit including a DC sense amplifier having a pair of inputs coupled to a pair of data lines and an output coupled to the external data terminal of the memory device; and

a multiplexer operating in a normal mode to couple the I/O lines for either the first or the second arrays to the pair of data lines, respectively, and operating in a test mode to couple the I/O lines for the first array to the data lines and to couple the I/O lines for the second array to the data lines.

42. The computer system of claim 41 wherein the memory device comprises a dynamic random access memory.

43. The computer system of claim 41, further comprising:

a first weak latch coupled to the first input of the direct sense amplifier;

a second weak latch coupled to the second input of the direct sense amplifier; and

combinatorial logic having a first input coupled to a first of the data lines and a second input coupled to a second of the data lines, the combinatorial logic providing an output signal indicative of a defective memory cell when both of the data lines are in the same logical state.

44. A method of testing a memory array comprising:

writing background data to the memory array;

coupling complementary digit lines for multiple columns in the memory array to inputs of a DC sense amplifier; and

simultaneously reading read data from multiple columns of the memory array.

45. The method of claim 44, further comprising generating an output signal from a NOR gate having inputs coupled to the inputs of the DC sense amplifier indicative of a defective memory cell when the inputs to the NOR gate are both logic "0."

46. The method of claim 44 wherein simultaneously reading read data from multiple columns of the memory array comprises simultaneously reading read data from multiple memory cells in different columns of the memory array where the multiple memory cells are collectively replaceable as a group by rows or columns of redundant memory cells.

47. The method of claim 44, further comprising replacing multiple memory cells, at least one of which was determined to be defective based on

simultaneously reading data from the multiple columns of the memory array, with redundant memory cells by blowing a fuse.

48. The method of claim 44 wherein simultaneously reading read data from the multiple columns of the memory array comprises:

reading first read data from a first column;

reading second read data from a second column;

compressing the first and second read data to provide compressed read data; and

generating an output signal indicative of a defective memory cell when the digit line and the digit line complement representative of the compressed read data are both logic "0."

49. A method for testing a memory array comprising:

storing background data in the memory array;

simultaneously reading read data from multiple memory cells in the memory array;

coupling the read data from the multiple memory cells to a pair of common complementary digit lines; and

detecting a defective memory cell when both of the pair of common complementary digit lines are in the same logical state.

50. The method of claim 49 wherein coupling the read data from the multiple memory cells to a pair of common digit lines includes combining the read data from multiple memory cells using a wired-OR interconnection.

51. A method for testing a memory integrated circuit comprising:

writing background data to memory cells in the memory integrated circuit;

coupling a first column of a memory array in the memory integrated circuit to inputs of a DC sense amplifier;

coupling a second column of the memory array to the inputs of the DC sense amplifier;

reading read data from a first memory cell in the first column; and

simultaneously reading read data from a second memory cell in the second column.

52. The method of claim 51, further comprising detecting that at least one of the memory cells in the first and second columns has failed when both digit lines coupled to the first and second columns are in the same logical state.

53. The method of claim 52, further comprising, when at least one memory cell is defective:

writing second background data to the first and second memory cells;

coupling the first column of a memory array in the memory integrated circuit to inputs of the DC sense amplifier;

reading second read data from the first memory cell;

determining if the first memory cell is defective;

coupling the second column of the memory array to the inputs of the DC sense amplifier;

reading second read data from the second memory cell; and

determining if the second memory cell is defective.

54. A method of combining data from multiple memory cells comprising:

writing background data to first and second memory cells;

reading the first memory cell to provide first memory data;

reading the second memory cell to provide second memory data;

combining the first and second memory data to provide compressed memory data such that when the first and second memory data disagree, both a first digit line carrying a signal representative of the compressed memory data and a second digit line that is normally the complement of the first digit line have the same logical state.

55. The method of claim 54 wherein combining the first and second memory data comprises wired-ORing of the first and second memory data.